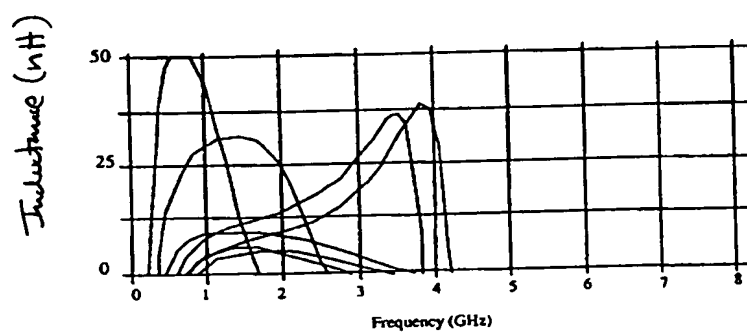


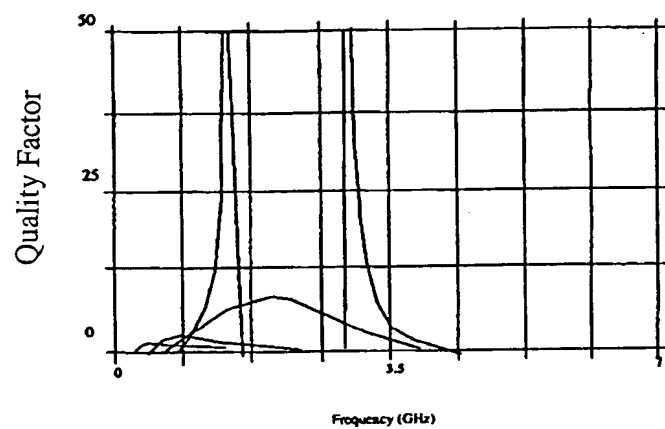
— 69 —

## FIGURE 2

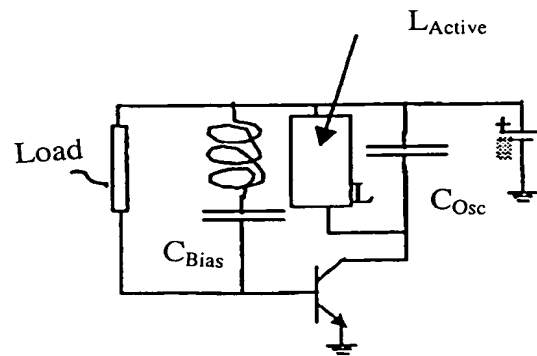
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**FIGURE 4**

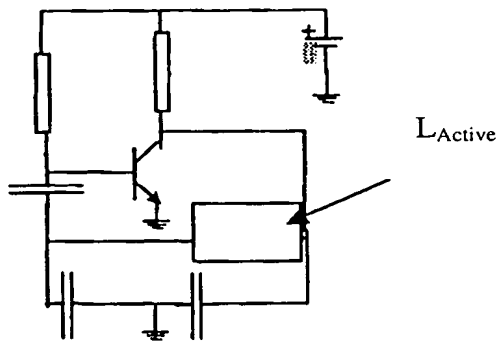


**FIGURE 5**

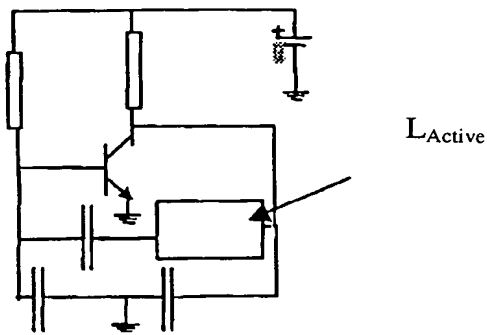


**FIGURE 6**

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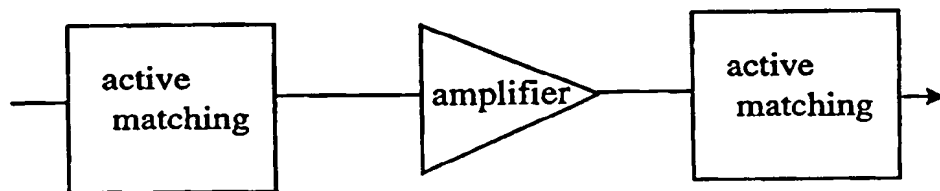


**FIGURE 7**

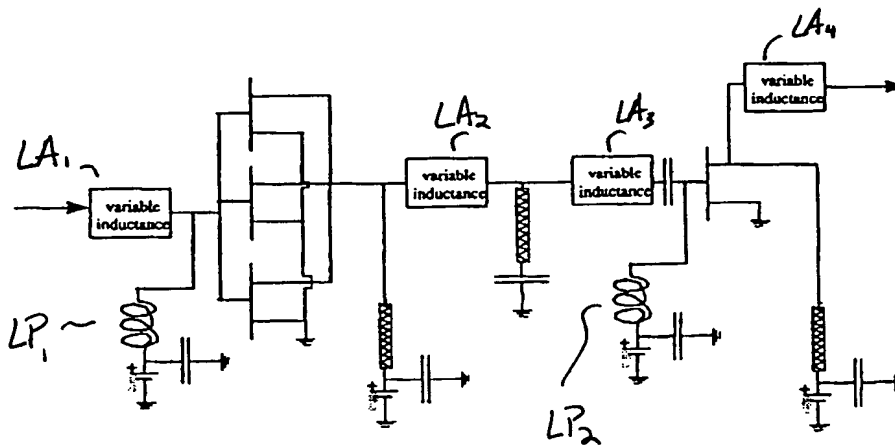


**FIGURE 8**

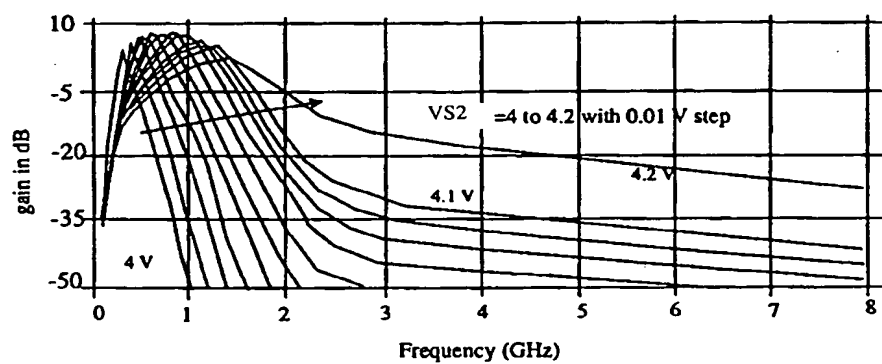




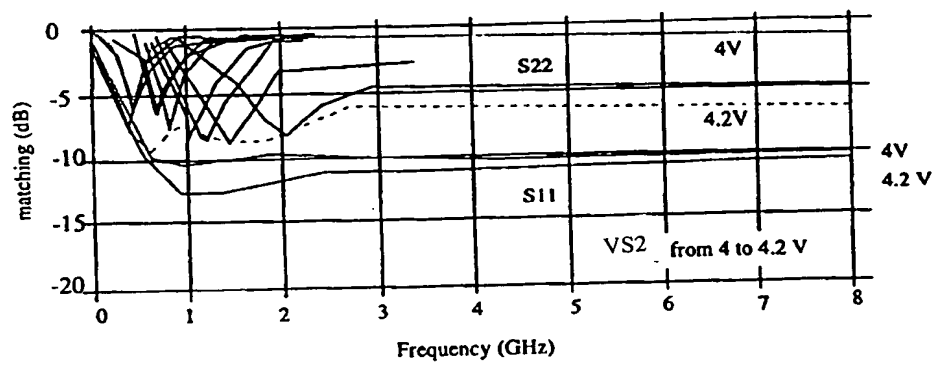
**FIGURE 9**



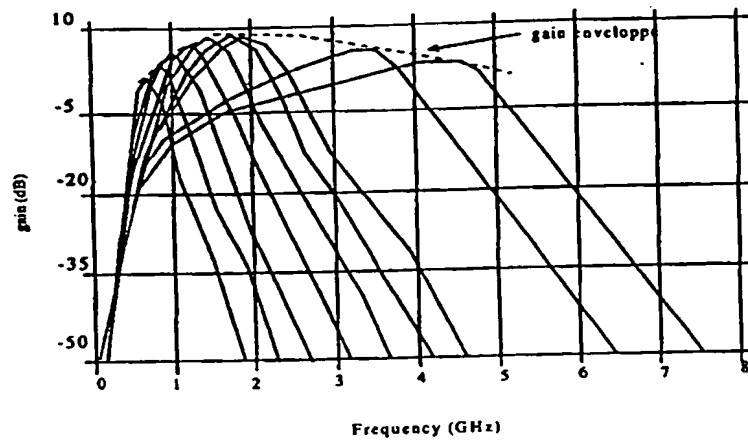
**FIGURE 10**



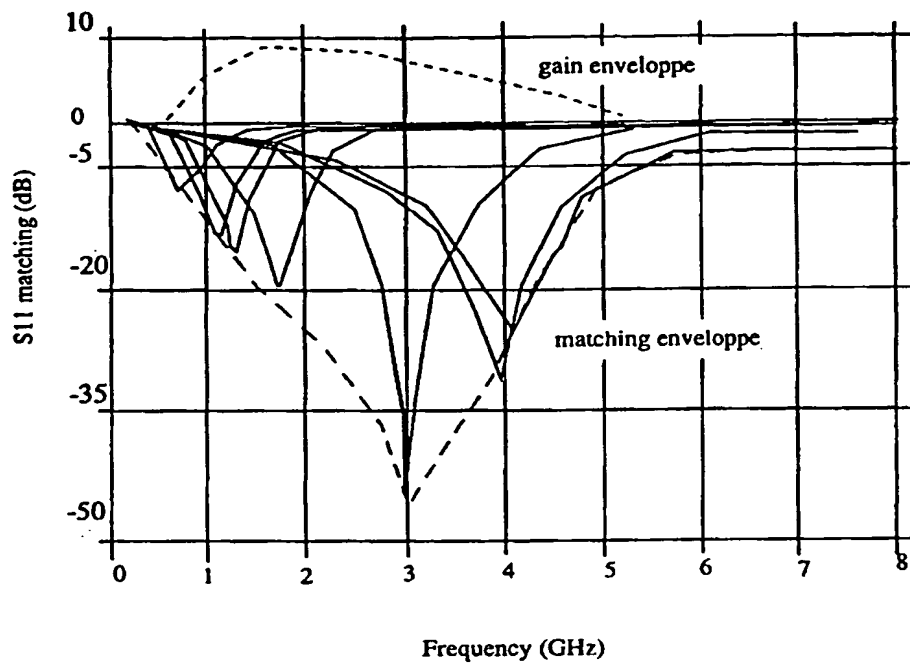
**FIGURE 11**



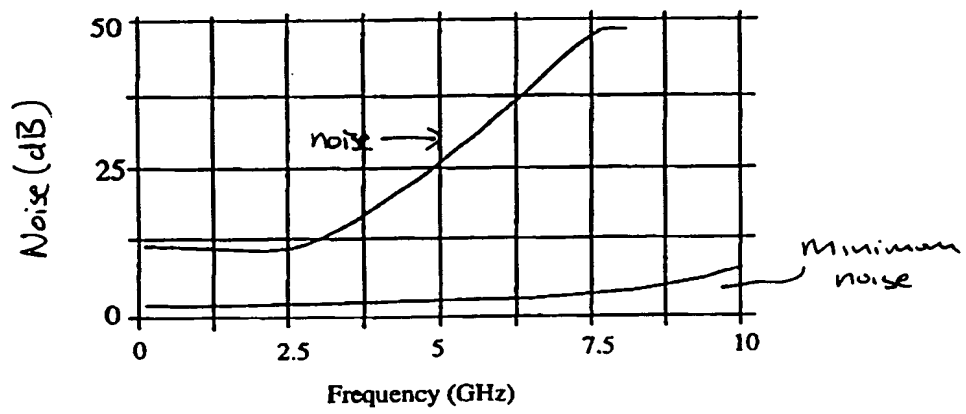
**FIGURE 12**



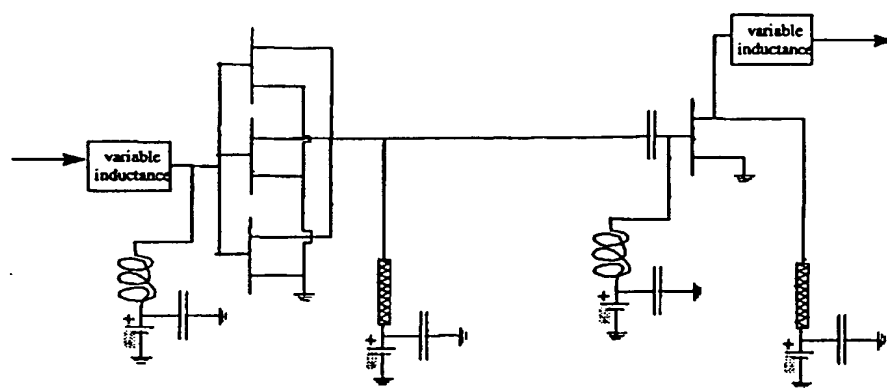
**FIGURE 13**



**FIGURE 14**

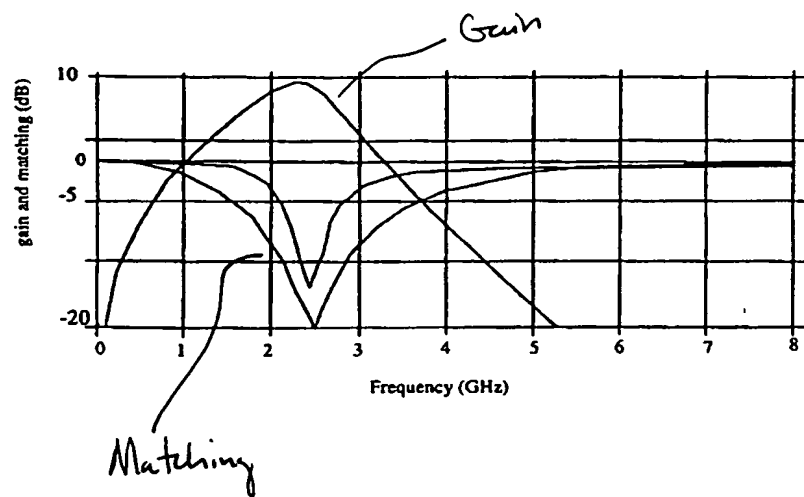


**FIGURE 15**



**FIGURE 16**





**FIGURE 17**

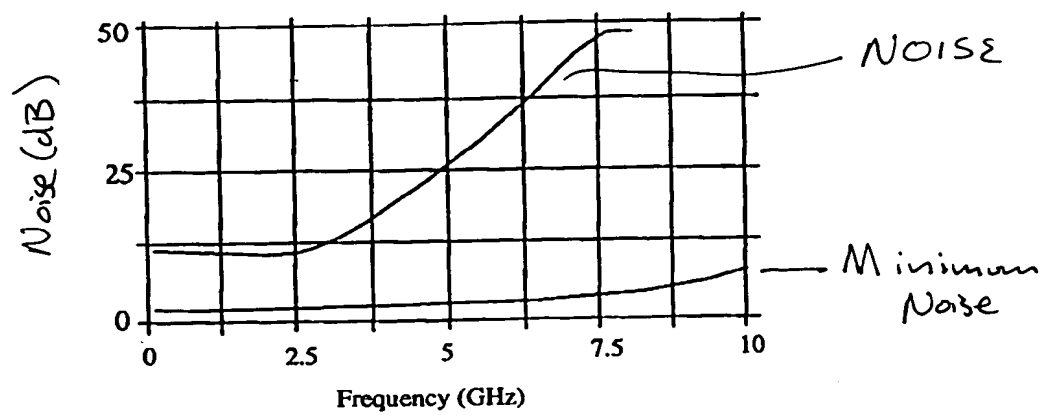
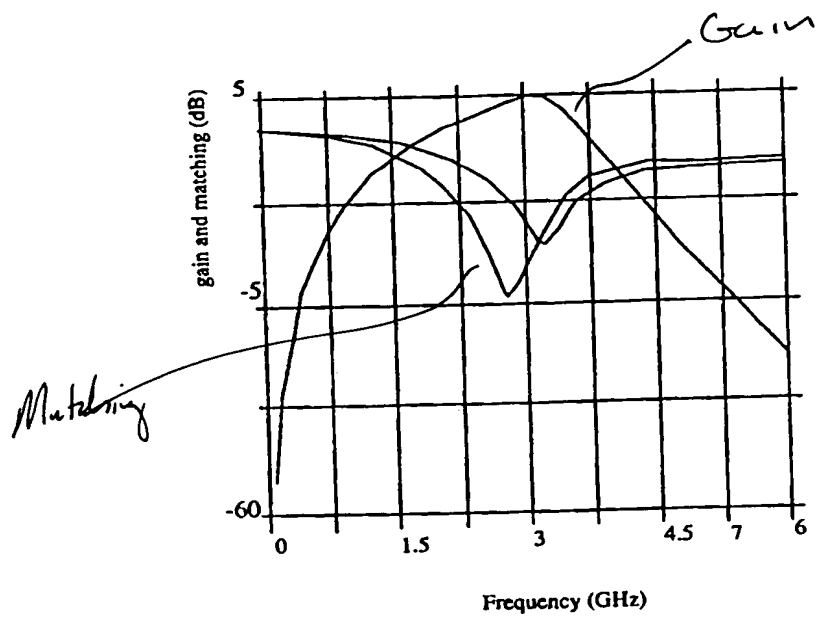
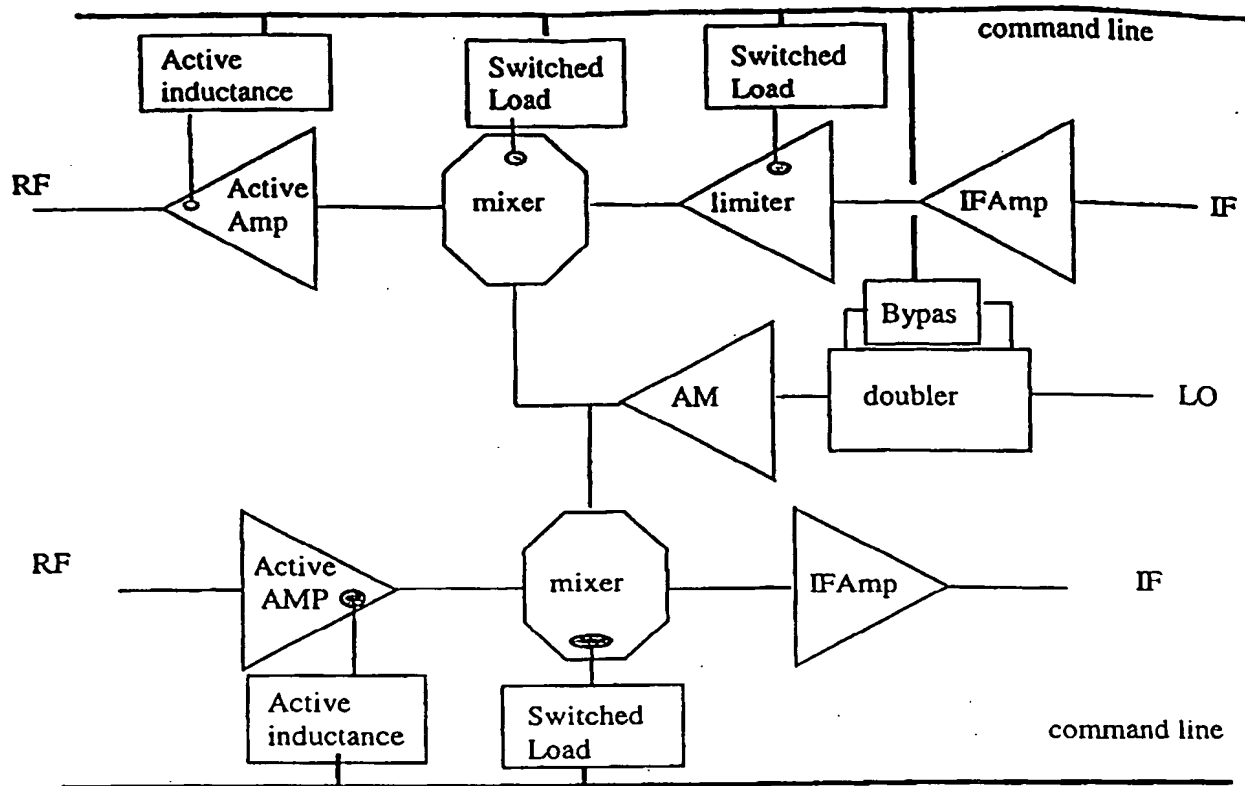


FIGURE 18

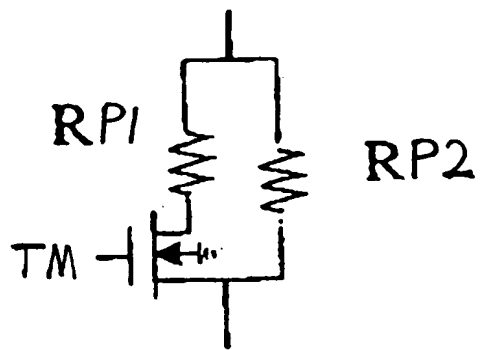


**FIGURE 19**



**FIGURE 20**

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**FIGURE 21**

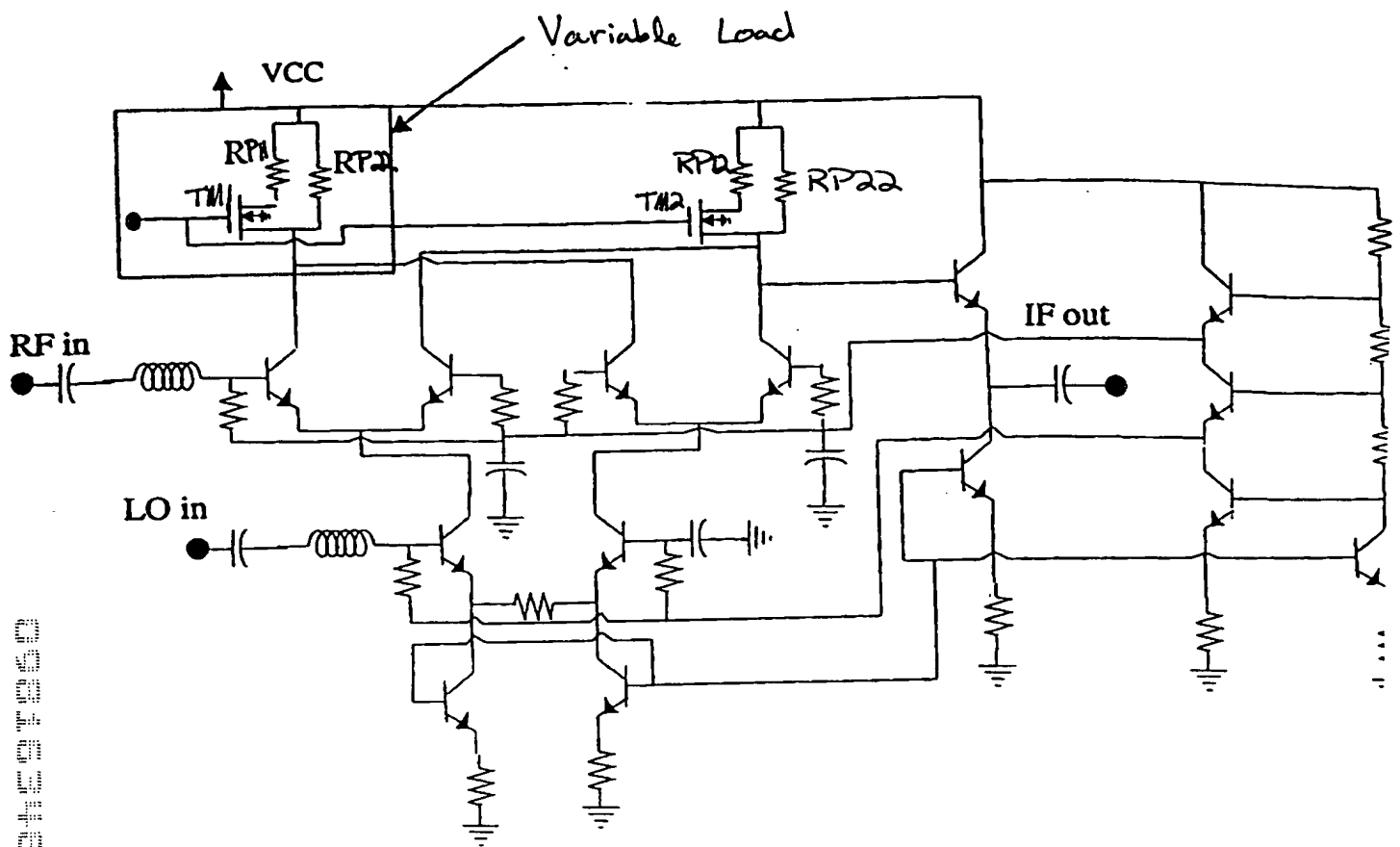
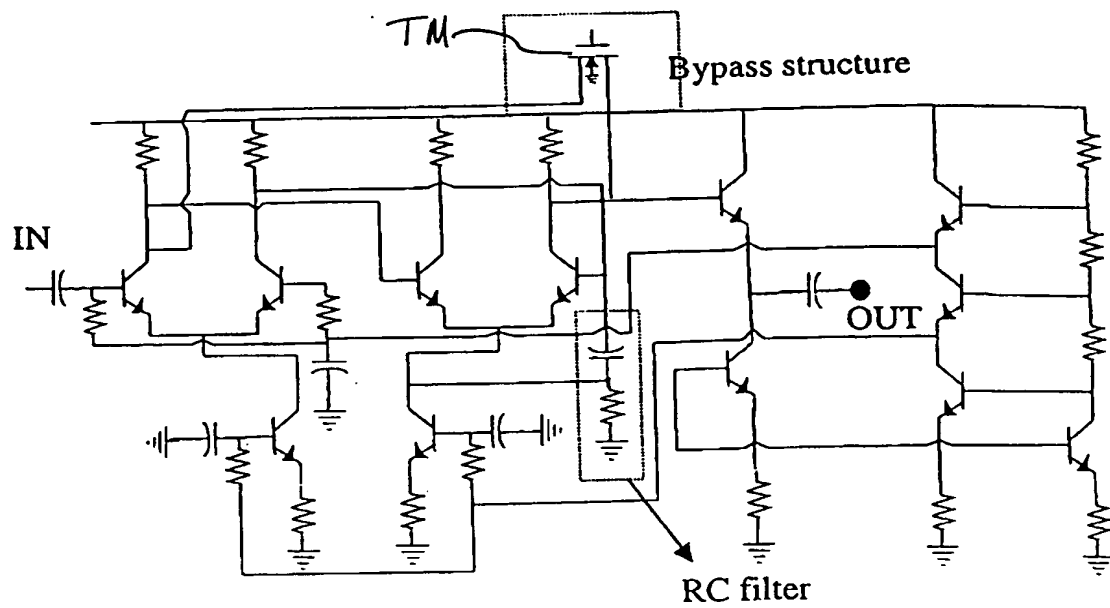


FIGURE 22



**FIGURE 23**

The diagram illustrates a three-stage CMOS amplifier. The first stage, labeled  $LA_{IN}$ , is a differential pair of NMOS transistors with a tail resistor connected to a bias voltage  $V_{G1}$ . The output of the first stage is connected to the gate of the second stage, which is a common-source amplifier. The second stage has a PMOS load resistor connected to  $V_{CC}$  and a tail resistor connected to a bias voltage  $V_{G2}$ . The output of the second stage is connected to the gates of the third stage, which is another differential pair of NMOS transistors. The third stage has a tail resistor connected to  $V_{CC}$  and is labeled  $LA_{OUT}$ . The output of the third stage is taken from one of the differential outputs.

**FIGURE 24**



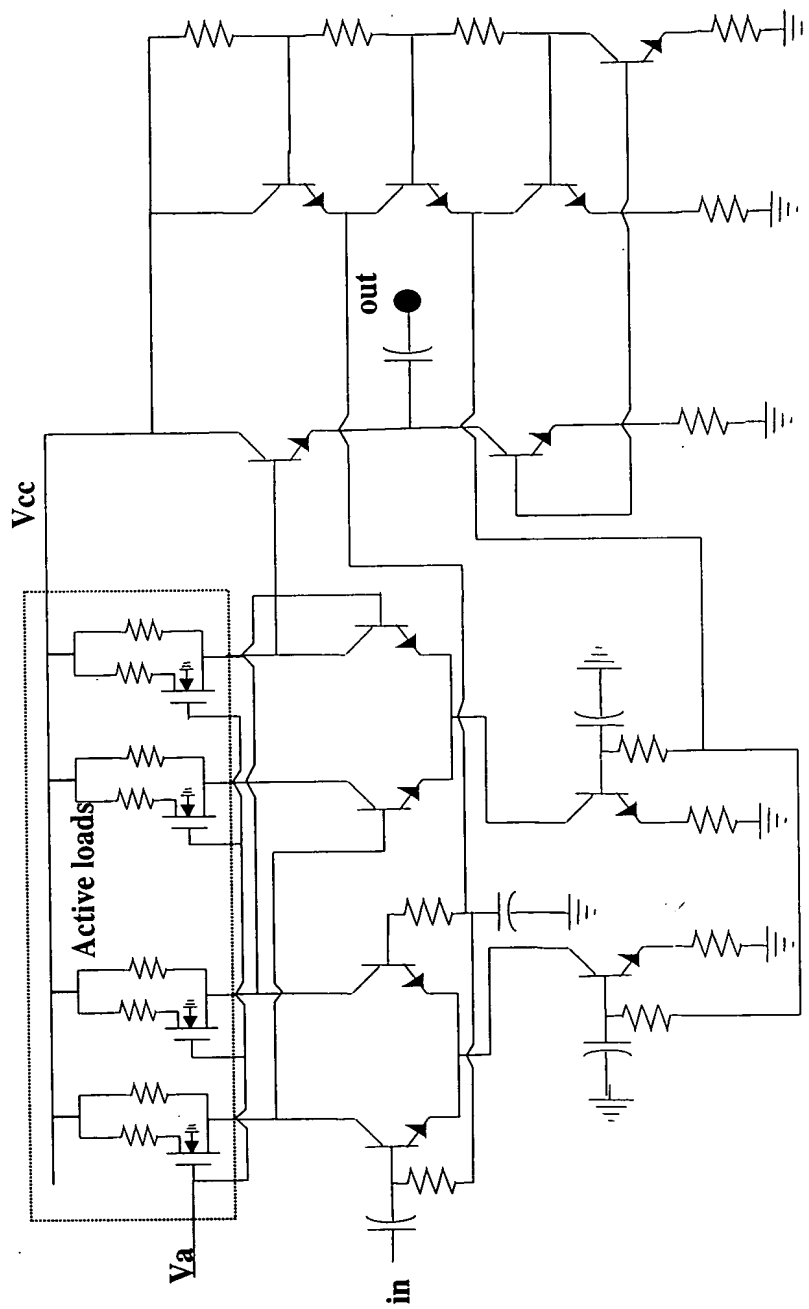


Figure 25